

INTEGRATION OF HIGH-K DIELECTRICS AND METAL GATES INTO SUBMICRON NMOS TRANSISTORS AT RIT. D. Jaeger, S. Kurinec*, *Department of Microelectronic Engineering, djj2950@rit.edu, skkemc@rit.edu*

Over the last 15 years MOS transistor performance has been improved by scaling the thickness of the silicon dioxide gate dielectric. In current CMOS technology, gate oxide thicknesses on the order of 12Å are being used for the 90nm node, with projections to scale the gate dielectric down to 8Å for the 65nm node. Continued scaling of the silicon dioxide gate will not be possible as it will soon be physically impossible to grow thinner silicon dioxide and direct tunneling will result in undesirable high off state leakage.

High permittivity (k) dielectrics offer a solution to achieve high gate capacitance at relatively larger physical thickness. In this study, the use of a high-k material as a replacement to the silicon dioxide has been investigated. The high-k material examined is zirconium oxide deposited by RF reactive sputtering. In addition to transitioning to high-k dielectrics, the scaled CMOS technology is also expected to replace polysilicon gates with metal gates as polysilicon gates suffer from gate depletion effects. Molybdenum, a refractory metal, has been investigated for the gate electrode, also deposited by RF sputtering.

These materials were characterized by fabricating capacitors and analyzing capacitance-voltage characteristics. Submicron NMOS transistors were fabricated using zirconium oxide as the gate oxide and molybdenum as the gate electrode, along with control devices with traditional materials for comparison. The transistors were fabricated using an existing submicron NMOS process recently developed at RIT with minor modifications. The transistors were tested for electrical performance. The results show the benefits and challenges of integrating high-k gate dielectrics and metal gates.