

HIGH TEMPERATURE CHARACTERIZATION OF III-V ON SI ESAKI DIODES

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In this study the temperature characteristics of GaAs/InGaAs tunnel diodes on Si substrates are reported. These devices are grown atop a virtual Ge substrate formed by a novel epitaxial growth technique known as Aspect Ratio Trapping (ART). At room temperature these devices outperform any prior reports of GaAs Esaki diodes on GaAs substrates in terms of the key figure of merit, the peak to valley current ratio (PVCR). In this abstract, we focus on device performance at temperatures of 20-200 °C. The PVCR of these devices reduces with temperature, however at temperatures above 100°C exhibit PVCRs in excess of 10.