CIRCUIT SIMULATIONS USING AN EMPIRICAL MODEL OF A GaAs ESAKI DIODE

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A record breaking GaAs Esaki diode, fabricated on top of a coalesced Ge Aspect Ratio Trapping (ART) substrate, has been modeled for circuit simulation. The simulations demonstrate the behavior of simple circuits at various temperatures. The results were compared to those obtained in studies conducted by Pawlik *et al.*.

The model developed is a modification of a pre-existing model, from S. M. Sze. The simple modifications made dramatically improve the accuracy of the model. The model uses the sum of 3 exponential terms; (i) a tunneling current, (ii) excess current, and (iii) diffusion current. A GaAs esaki diode was modeled using I-V measurements taken at temperatures ranging from 27 ^{o}C to 200 ^{o}C by Barth *et al.*. The final model was implemented into a simulation package, Gateway, which is distributed by Silvaco Data Systems Inc.

By comparing the simulation to the measured data, it was determined that the model is accurate. Various circuits were simulated such as (i) NOR gate, (ii) NAND gate, (iii) inverter, (iv) analog to digital comparator (ADC), and (v) tunneling static random access memory (TSRAM). The simulated characteristics were also compared to the results of a Si/SiGe device, as presented in the 2007 ISDRS by Pawlik *et al.*. It is noted that the GaAs device modeled for this work exhibits a large improvement in device and circuit performance.