Capacitance Voltage Analysis of High-K Dielectric on Strained Silicon

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As device dimensions shrink and technology pushes minimum device geometries beyond the 100nm node, new solutions beyond scaling will need to be found to continue to improve device performance. As devices are made smaller the short channel effects begin to degrade performance. By the introduction of a mechanical strain in the silicon the universal mobility of the free carriers can be increased, improving devices without the need for scaling. The purpose of this project is to investigate the CV response of metal insulator semiconductor (MIS) capacitors fabricated on strained silicon. For this purpose strained silicon wafers have been donated by AmberWave Systems. These substrates have been manufactured by epitaxially growing a relaxed $Si_{1-x}Ge_x$ layer on top of a silicon substrate. Next a silicon layer is grown on the Si1-xGex layer, with the lattice stretched inducing a biaxial strain in the silicon. For this investigation the MIS capacitors will be fabricated using a high-K dielectric, such as HfO_2.