Metal Source/Drain Schottky Field Effect Transistors and Schottky CMOS Circuitry

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***Abstract*—Field effect transistors in which the sources and drains are made of metal (aluminum), as opposed to silicon, have been conceived, designed, fabricated, and tested. For the n-body device, ambipolar operation is demonstrated, and two unique characteristics – leakage asymmetry and first quadrant negative differential resistance (NDR) – are identified and characterized. The p-body device failed, due to defect propagation through the gate dielectric. Additionally, critical issues involving real-world Schottky CMOS operation are identified for the first time, and a potential solution is proposed and discussed. The long-term goal of the presented work is 3D circuit integration, which is also discussed.**

***Index Terms*—3D circuitry, metal source/drain, MSD SFET, SBMOSFET, SBTT, Schottky CMOS, Schottky source/drain.**

I. Introduction

Over the past few decades, the drastic increase in consumer demand for smaller, faster, and cheaper computing devices has played a major role in driving the semiconductor industry to its current state, as well as increasing the range of applications for microprocessors. Quite naturally, however, new technologies pose new challenges. One such challenge is overcoming the degrading ability of aggressively-scaled transistors to act as desirable switches in digital circuitry, which has been running in parallel with overcoming the degrading ability to manufacture said transistors using conventional methods. Some solutions propose to scale devices in three dimensions rather than the current two (known as 3D circuitry for its suggestion of building multiple semiconductor levels on a single chip), while other solutions propose to better the performance characteristics of the devices themselves by utilizing unique processing techniques. It is the primary purpose of the Metal Source/Drain Schottky Field Effect Transistor (MSD SFET) to attempt to provide the potential for both such solutions with one [relatively] simple approach.

The MSD SFET was conceived as a means of implementing 3D circuitry in microelectronics in a cost effective manner. Regardless of the potential utility of MSD SFETs in 3D circuitry, however, further investigation suggests that the device may prove a potential candidate for future device scaling in traditional 2D CMOS.

The MSD SFET itself has sources and drains which are made of metal. With the right type of metal and the right type of semiconductor (i.e., n-type or p-type silicon of a particular doping level), a Schottky barrier is formed at the metal-semiconductor interface (a comprehensive analysis of metal-semiconductor junctions can be found in [1]). A gate is placed perpendicular to the source-body and drain-body interfaces, and modulates the barrier dimensions by accumulating or depleting majority carriers at the interface. In doing so, the interface effectively becomes more resistive or less resistive, thus resulting in a gate-modulated current flow.

Similar work has, coincidentally, been performed over the years using sources and drains made of metal silicides, some examples of which are in [2]-[9]. Metal silicides, however, are formed through diffusion of metal through silicon and some subsequent reaction to induce alloying. Since the MSD SFET design presented in this paper uses pure metal rather than metal silicides, this silicidation step is not necessary, and it may even be conceivable to use the same process level for both the NFET and PFET sources and drains as well as the first level of interconnects, thus decreasing manufacturing costs substantially. It turns out, however, that a combination of the use of silicides and the presented design may be a better approach, the reasons of which will be discussed later.

The primary advantage of the MSD SFET relative to conventional MOSFETs is that the source-body and drain-body junctions are ideally abrupt (e.g., no dopant concentration gradient exists), and so the device should be less susceptible to short channel effects such as DIBL and Vt rolloff. Additionally, the only implant step required is for the body region, thus eliminating the added cost of source/drain, LDD and halo implants. This implies no need for post implant anneals beyond the body implant, which means greater thermal process compatibility with high-k gate dielectrics.

II. THEORY

A. SBMOSFETs and SBTTs

Any given Schottky diode can be made to act in an ohmic manner by either using a semiconductor of the opposite doping (e.g., p-type vs. n-type), or by using a heavier-doped semiconductor. In the first case, the barrier height will decrease in value, and so the dominant current mechanism will be thermionic emission of carriers over the barrier. This is the principle of operation behind conventional

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SBMOSFETs (Schottky Barrier MOSFETs), where typically a n-Si body is used to make a Schottky barrier with PtSi, with a barrier height on the order of 0.85eV [1]. Inverting the body region to p-type decreases the barrier height to Eg-ϕ_{Bn}, or about 0.25eV. In the second case (using a heavier-doped semiconductor), the effect is that the band bending in the semiconductor at the metal-semiconductor interface increases, eventually to the point at which carriers have a high probability of tunneling through the sufficiently narrowed barrier. Therefore, in this case the dominant current mechanism is tunneling current. The effect of higher dopant concentrations can also be realized by accumulating or depleting carriers from the metal-semiconductor interface (with a gate bias) for a semiconductor of a given dopant level. Such is the principle of operation behind a different form of SBMOSFET, known as a SBTT (Schottky Barrier Tunneling Transistor).

Since conventional SBMOSFET operation relies on thermionic emission for the on state of the transistor, it is desirable for the source/body and drain/body barrier heights to be as low as possible under inversion to minimize contact resistance. This contact resistance can be expressed as [1]:

$$R_c = \frac{k}{qA^*T}\exp\left(\frac{q\phi_B}{kT}\right) \quad (1)$$

where k is Boltzman's constant, ϕ_B is the barrier height, T is the temperature, q is the charge of an electron, and A^* is the effective Richardson constant. Neglecting the temperature dependence of Rc, barrier height becomes the only variable which can be changed to affect the contact resistance in a conventional SBMOSFET.

For the SBTT, the on state takes place during high majority carrier concentrations, and so contact resistance can be expressed as [1]:

$$R_c = \exp\left[\frac{2\sqrt{\epsilon_s m^*}}{\hbar}\left(\frac{\phi_B}{\sqrt{N}}\right)\right] \quad (2)$$

where ħ is Planck's constant, m^* is the effective carrier mass, and N is the majority carrier concentration. While the same exponential dependence on barrier height is present, the contact resistance is effectively modulated by the gate bias, which accumulates or depletes carriers at the source/body and drain/body junctions. Therefore, the effect of larger barrier heights can be countered by stronger accumulation. It should be noted that under very strong inversion in SBMOSFETs, tunneling current becomes significant, at which point the conditions in (2) are applicable. Also, if the inversion mode barrier height in a SBMOSFET is not very low, then it should essentially act as a SBTT (inversion mode barrier height can be expressed as the difference between the semiconductor bandgap and the equilibrium barrier height).

Considering that both conventional SBMOSFETs and SBTTs start from the same device, and that the only difference between the two is the polarity of the gate and drain biases, it would not be unreasonable to suggest that a transistor with Schottky sources and drains would exhibit both conventional SBMOSFET-like and SBTT-like characteristics with the appropriate biases at each terminal. This characteristic is known as ambipolarity, and is indeed present in any transistor with Schottky source/drain regions. The ambipolarity characteristic poses potential difficulties in implementing Schottky CMOS; however, this is discussed in more detail later in this paper.

B. MSD SFETs

The MSD SFET (SFET for short) was initially meant as a form of SBTT, in that switching takes place through accumulation (and so tunneling current dominates the on state current). For the devices reported in this paper, it is only the n-body SFET which acts as a true Schottky transistor, as the goal is to implement CMOS circuitry by using one metal instead of two separate metals for two separate Schottky barriers for n-Si and p-Si. Since this design uses a n-Si body for the NFET, the PFET uses a p-Si body, and so a Schottky barrier formed with the source/body and drain/body junctions in the NFET is either Schottky but with a lower barrier height or simply ohmic for the PFET. With zero gate bias, then, the PFET is in the on state and must be switched off through depletion. To utilize such a PFET in CMOS circuitry, however, the device would need two non-independent gates in a FinFET-like configuration, whereby the body width is less than twice the maximum gate-induced depletion width.

C. MSD SFET with a Drian Bias

In a conventional MOSFET, pinchoff occurs when the difference between the drain bias and gate bias is small, such that the channel region near the drain is no longer inverted. This results in the saturation region in the Ids vs. Vds characteristic. The mechanisms behind saturation in the SFET are very different.

At zero drain bias, and for any gate bias, some sort of band bending takes place at the source-body and drain-body interfaces. For a n-body SFET with a positive drain bias, the drain-body diode is forward biased (and so the "barrier height" is the built-in voltage of the diode) and the source-body diode is reverse biased (the barrier height is that on the metal side of the junction). As a drain bias is applied, the built-in voltage of the drain-body diode decreases by $V_{bi} - (V_{drain} - V_{body})$, and eventually this diode will turn on much like a standard p-n diode. However, even in the "on" state, the drain current is limited by the source current, and the source-body diode current is the reverse bias saturation current (for a given source barrier width, there exists a limit as to the number of carriers that can be injected from the source into the body). At low drain biases, the maximum source injection current is relatively constant, and not being utilized to full capacity, thus resulting in the linear region of the Ids vs. Vds plot characteristic. At Vd_{sat}, the maximum number of carriers are injected from the source for the specific source barrier width, and within some region afterwards increasing the drain voltage will result in little if any increase in drive current. It is at this point that the transistor is in the saturation region of operation.

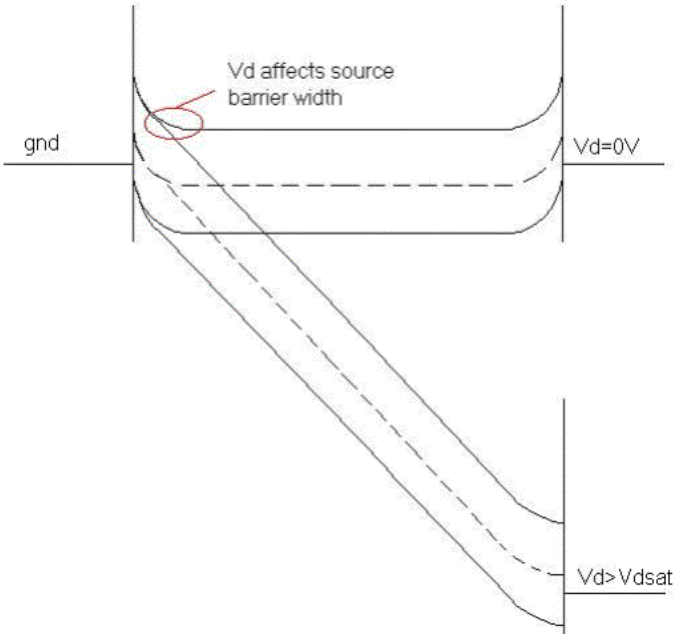

Fig. 1: Metal-semiconductor-metal energy band structure at Vd=0V and Vd>0V for a given gate bias. The drain bias decreases the source-side barrier width, while simultaneously decreasing the built-in voltage of the drain-body diode. This effect has been coined as Drain Induced Source Tunneling (DIST), and becomes significant at very high drain biases.

As Fig. 1 shows, at drain biases well beyond Vd_{sat}, there is enough of a lateral field throughout the transistor such that the drain has control over the source barrier width. At this point, the maximum source carrier injection current increases with drain bias, and this injection current is fed to the drain-body diode which, at such high biases, is already in an "on" state. This results in a diode-like I-V behavior at very high drain biases. Increasing the gate bias will decrease the source barrier width, thus increasing the lateral field required to further decrease said barrier width. At higher gate biases, then, the drain voltage at which DIST occurs is increased (shown later in Fig. 17).

It should be noted that this description of the DIST effect treats the device as a MSM device without a gate. This is a reasonable assumption for negative drain biases in a n-body SFET (though the tunneling is then at the drain end), but under positive drain biases, with the gate grounded, the body region near the drain is inverted. An added effect apart from DIST takes place, then, whereby holes are injected from the drain. For large barrier heights to n-Si, this effect drastically increases the leakage current at positive drain biases, resulting in leakage current asymmetry about the y-axis. Low barrier heights to n-Si reduce hole injection from the drain, as the inversion mode barrier height is increased.

Real-world Schottky diodes also experience some change in the barrier *height* as a function of the field across the diode, due to the sum of the image field and the real field. This is another factor in DIST, as the barrier height in the reverse-biased source/body diode decreases with increasing reverse bias, thus increasing the likelihood of thermionic emission current.

While DIST is something of an undesired effect, it can be engineered to not interfere with device operation inside a particular voltage range. If the body region has a high doping level, then the barrier width becomes small, and thus requires a large lateral field to shrink it further. Large body doping levels therefore increase V_{DIST}, the drain voltage at the onset of DIST. The tradeoff, however, is an increase in off state leakage at drain voltages below V_{DIST}, as the tunneling probability for majority carriers is increased.

D. MSD SFETs on SOI Substrates

If SOI substrates were used to manufacture SFETs, it should be expected that the SFET would experience little if any floating body effect (which correlates to the "history effect"). First considering the n-body SFET, the reverse-biased diode is the source-body diode (for positive gate and drain biases). Applying a drain bias with zero gate bias should result in little charging of the body region, as the majority carriers (electrons in this case) must first traverse the *source*/body junction. Since Schottky diodes are majority carrier devices, in the case of the n-body, n-channel SFET, only electrons may enter the body region and bring it to some potential. Whichever carriers do end up traversing the source/body junction are immediately swept through the drain, as the forward bias turn-on voltage for Schottky diodes is typically very low. In the negative drain bias case, the same conditions apply, except that now the drain/body diode is the reverse biased diode. SFETs, or any Schottky transistor, should therefore be immune to the floating body effect for both parts of their ambipolar operation.

The p-body FET used in this experiment is not a SFET, but more like a gate-modulated resistor – it starts off as having ohmic contacts at the source/body and drain/body interfaces, and the device is switched off when the gate "blocks" current flow between the source and drain. When the p-body FET is in the off state, the body region in contact with the source/drain regions is depleted. In such a case, no net carrier concentration exists, and so the body region cannot charge up to some potential.

At this point it is important to note that one must not confuse leakage current with current that results in a floating body effect, as the two are not necessarily the same. In conventional SOI MOSFETs, the floating body effect occurs from majority carrier injection into the body via impact ionization or injection from the drain. In such a case, if the energy barrier at the source-body junction is relatively large, these carriers are "stored" in the body for some period of time, thus decreasing the threshold voltage (for partially depleted, or PDSOI, devices). This leads device designers to a "fork in the road," whereby they can either design the device for minimal leakage current (extremely difficult for high speed operation), or they can induce defects at the source-body junction to allow injected carriers to leak away, thus decreasing the carrier storage time in the body (but this has the added effect of increasing leakage current, thus decreasing Ion:Ioff). In short, for the most part at least, this should not be the case in SFETs, as injected carriers from the reverse biased diode are immediately swept away by the forward biased diode.

The implications for a floating body effect, or lack thereof, are very important to take note of, as the floating body effect is considered to be a primary disadvantage regarding circuit design on SOI substrates (due to the resultant dependence of the threshold voltage on the body potential, which is not constant throughout a clockpulse). That the body region of a SFET should not float to a potential allows one to utilize the advantages of SOI technology without the challenge of taming the history effect.

E. 3D Circuit Integration

The notion of 3D circuitry, by which multiple device layers are stacked on top of each other within a single chip, has been around for some time, with efforts performed by various research groups [11]-[18]. These implementations, however, utilize conventional MOSFETs. Likewise, as of yet SBMOSFET and SBTT research has not hinted at applications to 3D circuit integration. Considering the possibility of Schottky CMOS becoming a placeholder on the ITRS roadmap towards the end of CMOS scaling [19], integration of Schottky CMOS into 3D circuitry would seem a natural progression.

The real strength of 3D circuitry is not that individual logic gates can be built using multiple levels (thus consuming less area), but rather that entire logic *branches* can be built on multiple levels, and that this can be exploited to minimize transmission delays through interconnects. For example, an ALU unit in a microprocessor can be built with three device levels, thus consuming less area. Or, perhaps, the ALU can be built on one level and the SRAM can be built directly on top on another level. With enough levels, it might also be feasible to realize solid state hard drives which operate much faster than the mechanical units in present day computer systems. The potential for maximizing packing density is quite staggering, as are the implications for System-on-a-Chip (SoC) solutions.

Some approaches to 3D circuit integration involve chip-to-chip or wafer-to-wafer bonding. This is effective in that it realizes single-crystalline silicon for each device level, thus maximizing performance. The temperatures required for the bonding techniques are low enough so as not to significantly affect the performance characteristics of the fabricated devices. However, that n separate chips must be manufactured to build a n-level 3D circuit results in the final product costing roughly n-times as much. This clearly raises practicality issues for large volume, low-cost fabrication. For high-end systems where cost is not a concern, however, it may well be the best solution. SFETs are particularly advantageous in the wafer-to-wafer approach, at the very least from a cost standpoint. Since the SFET is a much simpler device to fabricate than a conventional MOSFET, and therefore costs less to fabricate, this cost differential may be enough to minimize the added cost of successive device levels in 3D circuits.

Another approach to 3D circuit integration is to deposit silicon films on top of previous device layers. This allows a multi-level "chip" to be fabricated on a single wafer, presumably reducing manufacturing cost. The deposited silicon film is recrystallized to form a polysilicon film of some grain size, on which devices are fabricated. The disadvantage to this process is that, by virtue of the devices being manufactured on polysilicon films as opposed to single crystalline silicon films, the devices themselves exhibit poorer performance characteristics due to degraded carrier mobility and increased leakage currents. However, if the grain sizes can be made large enough such that one device, or one logic gate, or perhaps an entire logic branch, can be fabricated within a single grain, then the device performance in such large grain polysilicon films is equivalent to that of single crystalline silicon.

One of the more promising methods for recrystallization of deposited silicon films to large grain polysilicon is known as MILC (Metal-Induced Lateral Crystallization) [14], [15]. Normally, recrystallization takes place vertically, and so the grain size is on the order of the film thickness. For aggressively scaled devices, this is not desirable, as thinner silicon films are becoming necessary to maintain or improve performance. The MILC process uses nickel "trenches" between areas of amorphous silicon. At elevated temperatures, the nickel forms a silicide and diffuses *laterally* through the amorphous silicon, leaving large grain polysilicon in its wake. Further recrystallization takes place at higher temperatures (albeit over less time). Two level 3D circuits built using this method have been shown to exhibit enhanced performance over 2D SOI circuits [14]. However, the primary issue is that recrystallization takes place over very long periods of time (tens of hours), and at temperatures which may affect device performance (~600-900°C).

Another issue regarding MILC is that of varying crystal orientation. Even though it is possible to fabricate devices, or logic gates, or logic branches within a single polysilicon grain, the crystal orientation of that grain is not guaranteed to have particular Miller Indices. Therefore, the channel mobility varies from device to device on a given die, thus introducing statistical device performance distributions which only add to the inherent distributions that are a result of discrete dopant effects in aggressively-scaled devices. This, in effect, makes high performance circuit design more difficult.

A significant challenge to any approach to 3D circuit integration is yield, as yield issues are compounded with each device layer. If, for example, a 3-level 3D circuit is built using wafer-to-wafer bonding, with each wafer yielding 80%, then the final yield is on the order of 51%. Therefore, for any approach to 3D circuitry, it is critical to achieve very high intra-level yields to realize an acceptable final yield.

The most significant challenge to 3D circuit integration, however, is thought to be the optimization of vertical interconnect routing [15], rather than the deposition/formation of single crystalline or near single crystalline silicon films. The SFET can be useful for 3D circuit integration in that, in the design presented, the device is more comparable to a switch within the interconnects (PIW – Processing In Wire, in this respect similar to QCA [20]) than the current day perception of devices separate from the interconnects. This in itself has potential for increased 2D packing density, but also has increased potential to overcome device contact issues (also for 2D circuits) at very small sizes, as well as interconnect routing issues for 3D circuits (the simplicity of

the device layout should allow more freedom in circuit design). The SFET (or any Schottky transistor), therefore, may prove a universally useful device for both 2D and 3D circuitry, if not for its potential performance advantages [2]-[9], [21], [22], then at the very least because of its simplicity and cost of fabrication.

F. Schottky CMOS

It was mentioned previously that Schottky CMOS can be difficult to implement because Schottky source/drain devices are ambipolar. This is a point that is often not made in discussions of Schottky CMOS and/or Schottky source/drain devices, as in such discussions only inversion mode operation is considered [21], [22]. To date, real-world Schottky CMOS operation has yet to be demonstrated. Additionally, in such discussions, the "NFET" source/drain regions are made of $ErSi_2$, and the "PFET" source/drain regions are made of PtSi, which result in large barrier heights (and consequently, low inversion-mode barrier heights) to p-Si and n-Si, respectively. While PtSi and $ErSi_2$ would provide for the best performance for n-body and p-body devices, respectively, the use of both materials is not required because of each device's ambipolarity (e.g., a Schottky "PFET" is really not a PFET, as it can also act as an NFET).

In order to better understand the implications of ambipolarity, first consider the pull-up network a conventional CMOS inverter. In the inverter, the drain of the pull-up network (PFET) is at a positive bias, which results in a negative gate-to-body bias as a function of position across the channel. The positive V_{DD} value, then, acts as a negative gate bias, inverting the PFET body region such that the PFET is in its saturation mode of operation (with a large enough V_{DD}). There is an important observation here, in that in the low input state, current flows through the PFET with zero gate bias.

To build an inverter with Schottky transistors, and to operate it in the same fashion as conventional CMOS, would require additional tact. This is because metals do not have a valence band or a conduction band, and so the energy level of carriers in the metal source/drain regions is on the order of the Fermi level in the metal, which means that carriers must either tunnel through the Schottky barrier via the field from the drain bias or possess enough thermal energy to surmount it. With a Schottky "PFET" (n-body), a positive V_{DD} value inverts the body region, much like a conventional MOSFET, thus bringing the inverter output to V_{DD} via hole thermionic emission. One must take caution, however, in engineering DIST such that $V_{DD}<V_{DIST}$ for the pull-down network. If V_{DD} is too large, then drain-to-body tunneling leakage in the Schottky "NFET" becomes significant and the inverter output is lowered. Even for $V_{DD}<V_{DIST}$, however, the pull-down network can still turn on, as the positive drain bias, when coupled with the gate, accumulates holes at the drain/body interface. This decreases the barrier width at the drain, thus placing the pull-down network in accumulation mode operation. The output of the inverter is therefore lowered.

Additionally, turning the pull-up network off becomes a significant challenge. With the "PFET" in saturation mode, pinchoff occurs at the source end of the transistor, which means that the net carrier concentration (and hence the difference between the conduction band and the Fermi band) decreases from the drain to the source. When the inverter input is raised to V_{DD}, the expected result of a decrease in hole injection from the drain occurs; however, at the same time electrons are accumulating at the source/body diode, thus lowering the barrier width. Therefore, the decrease in drain/body hole injection results in an increase in source/body electron injection. In other words, the ambipolar Schottky "PFET" has switched from inversion mode operation to accumulation mode operation. This raises the inverter output value.

The combination of the pull-down network turning on at zero inverter input, and the pull-up network not turning off at a logic high inverter input, becomes a serious issue. It is critical, therefore, to design Schottky CMOS circuitry in a manner that circumvents these issues in a tactful manner, either by controlling device ambipolarity or by taking advantage of it. The author has formulated several approaches for this, one of which is the design presented in this paper – with a p-body pull-up network, and using the same metal as the n-body pull-down network, the p-body device should be in an "on" state with zero gate bias. Applying a positive input to the inverter will deplete the p-body region, thus cutting off source-to-drain current in the pull-up network, while at the same time putting the pull-down network into accumulation mode operation. Since the pull-down network has a n-type body rather than a p-type body, with a low workfunction gate (such as Al) and positive V_{DD} values the challenge of keeping the pull-down network off for zero inverter input can be minimized.

III. EXPERIMENTAL PROCEDURE

The devices were fabricated on 4-inch 15Ω-cm bulk n-Si wafers with aluminum as the metal of choice. Aluminum was chosen because it is relatively simple to manufacture Schottky diodes using aluminum and lightly doped n-Si. A top-down view and two cross-sections of the MSD SFETs are shown in Figs. 2, 3, and 4, respectively. The manufacturing process requires seven lithography levels. Level 1 defines the N+ implant which acts as an ohmic contact to a Al/n-Si Schottky diode. Level 2 defines the p-well implant, which is used for the p-body device. Both implants are performed through a 500Å dry pad oxide, and the anneal/drive-in process uses the same pad oxide recipe. The resulting ~1000Å of oxide serves as a field oxide, through which active areas are defined and etched (Level 3). The exposed silicon surface is put through a pre-evaporation clean (1 min. dilute HF, 1 min. DI rinse, N2 blow dry), and then placed in a bell jar evaporator for pure aluminum deposition (wafers under vacuum in 5-10 min.). Evaporation took place in the low E-6, high E-7 Torr range.

Level 4 defines the metal source and drain as one piece. The photoresist is left on the aluminum, and a silicon etch is performed using SF_6 and CHF_3. The photoresist is then stripped, and a channel define etch is performed which splits apart the source and drain regions (Level 5). The gate dielectric (500Å PECVD TEOS) is then deposited and patterned (Level 6), as is the second layer of aluminum, which acts as the gate electrode (Level 7).

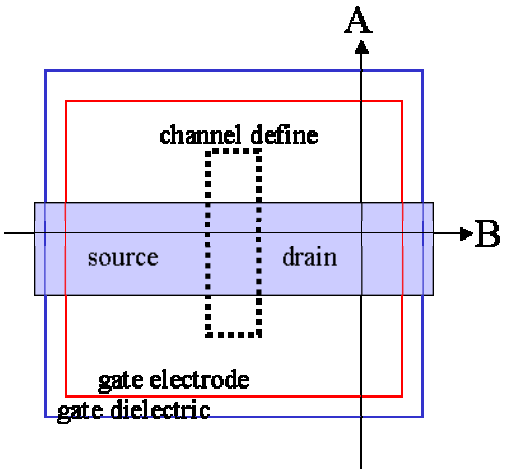

Fig. 2: Top-down view of MSD SFET with cross-sections A (Fig. 3) and B (Fig. 4).

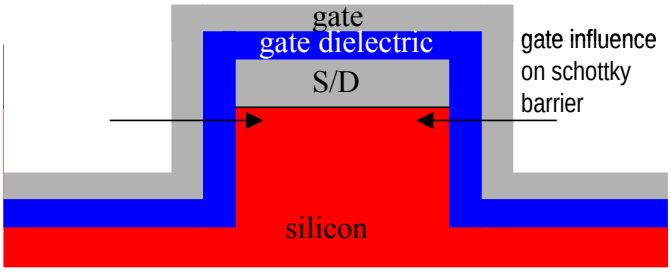

Fig. 3: Cross-section A of Fig. 2.

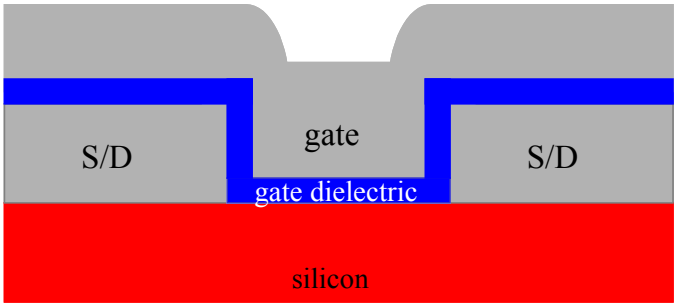

Fig. 4: Cross-section B of Fig. 2.

In various stages of the process, different wafers were sintered at 450°C in H2/N2 forming gas for 15 min. It was unclear at which point in the process would be the best point to perform a sinter so as to ensure the best device operation, or any device operation, so these three splits were performed. As will be shown later, however, it turns out that there is no appreciable difference between the sinter splits. SFETs were manufactured on a total of nine wafers, with four processing splits, as defined in Table 1. One wafer from each of the splits was run through the entire 7-level process to fabricate both n-body and p-body devices (as well as test structures), while the other six wafers went through a 6-level process for the n-body devices and test structures.

TABLE 1

MSD SFET Process Splits

Wafer number	Split definition
2,3,4	Post M1 deposit sinter (Split 1)
5,6,7	Post silicon etch sinter (Split 2)
8,9,10	Post channel define sinter (Split 3)
2,6,10	P-well implant for p-body FETs

IV. EXPERIMENTAL RESULTS AND DISCUSSION

Fig. 5 shows the "burn-in" process performed on a n-body SFET. The purpose of the burn-in process is to fill in as many surface states at the metal-silicon interface as possible. This allows for greater consistency when comparing the results of various devices. The device tested in Fig. 5 achieved a sufficient burn-in after 14 iterations. The best number of burn-in iterations, however, tends to vary from device to device, as do the burn-in characteristics. Minimization of surface states, therefore, is a major challenge regarding using metal-silicon junctions for Schottky CMOS. Metal silicide-silicon junctions, however, should not have this problem, at the very least because no burn-in process is reported in [2]-[9]. Another significant challenge with using pure metal is the development of a self-aligned gate technology, for which, once again, silicides do not have this problem as they are diffused rather than deposited. A combination of the advantages of metal silicide source/drain regions and the layout advantages of the design presented, which is essentially a FinFET with silicide source/drain regions, may prove to be the best solution. Such a device is currently a work in progress by the author.

Fig. 6 shows the complete Ids vs. Vds characteristic of the same device for both accumulation mode and inversion mode operation, as predicted from the theory section. Figs. 7 and 8 show the Ids vs. Vgs characteristic for the same device in accumulation mode and inversion mode, respectively, and Figs. 9-11 show the same plots as Figs. 6-8, but on a different die tested two months after the device in Figs. 5-8. Although the same exact device was not tested, the trend in the data is consistent between die and wafers, and so is somewhat representative of the time-dependent change in performance characteristics of the device in Figs. 5-8. Absolute current is used in all of the presented figures, as the true current density is unknown – for this particular design, the device width is not the same as the channel width, as the channel is on the sidewalls of the silicon fin.

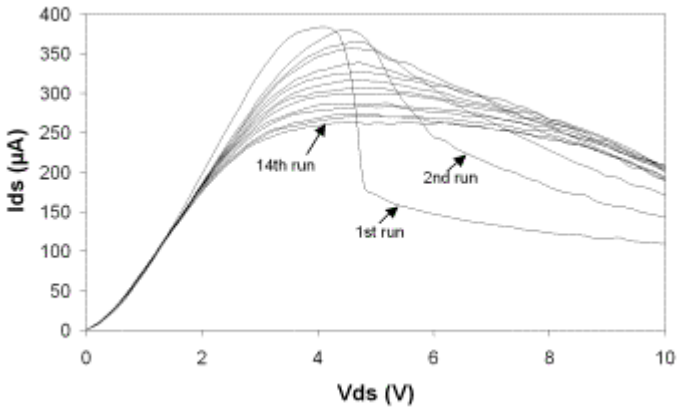

Fig. 5: Ids vs. Vds "burn-in" process of 14 runs for an n-body SFET (Wmask = 5μm, Lmask = 2μm, Wreal = 3.24μm, Lreal = 4.11μm) from Wafer 6. The gate is kept at 10V and the drain is swept from 0V to 10V until the resultant curve becomes repeatable. It is also possible to perform an inversion mode burn-in; however, this degrades the performance of the device (though a subsequent accumulation mode burn-in recovers the performance). The decrease in drive current per iteration may be due to the repulsive force of trapped charge at the M-S interface.

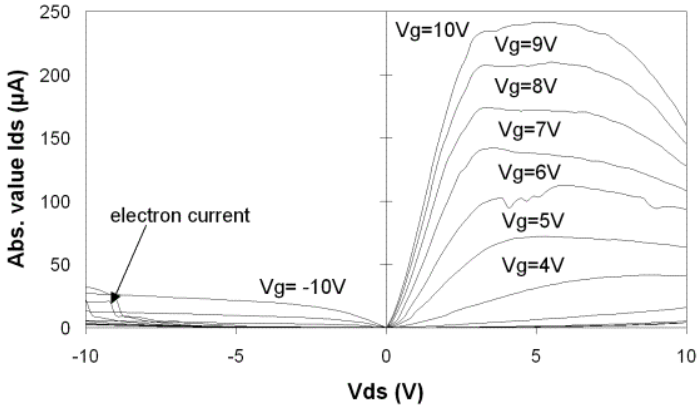

Fig. 6: Absolute value Ids vs. Vds characteristic for 2μm x 5μm n-body SFET from Wafer 6. Peak current in the first quadrant is 242μA, and 27μA in the third quadrant. The asymmetry in leakage current between first and third quadrant operation will be discussed later. The negative differential resistance (NDR) region in the first quadrant at high gate and drain biases is due to an increase in the source/body barrier width, which decreases the electron tunneling component of the on-state current. This will also be discussed later.

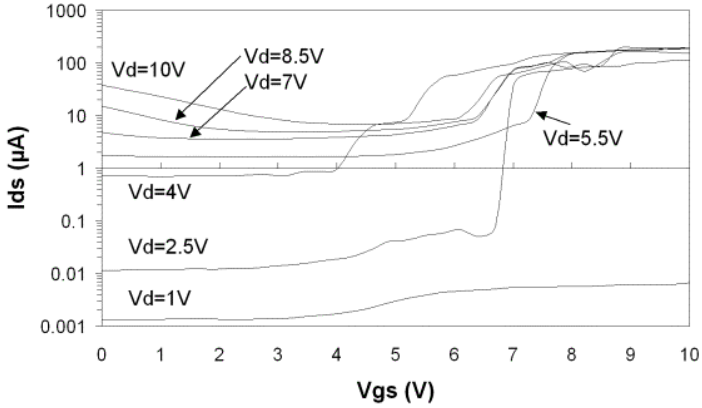

Fig. 7: Ids vs. Vgs characteristic for 2μm x 5μm n-body SFET (n-channel). Vds was varied from 1V to 10V in 1.5V increments. Ideal operation looks to be in the Vds=2.5V range, which exhibits the lowest sub-threshold slope (111mV/dec.) and highest Ion:Ioff (3.99 dec.).

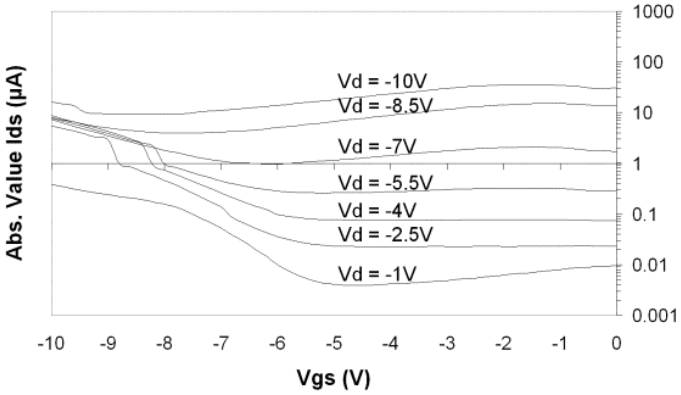

Fig. 8: Absolute value Ids vs. Vgs characteristic for 2μm x 5μm n-body SFET (p-channel). Vds was varied from –1V to –10V in –1.5V increments. Ideal operation looks to be in the Vd = -1V to –2.5V range, although the sub-threshold slope and Ion:Ioff are poor relative to accumulation mode operation.

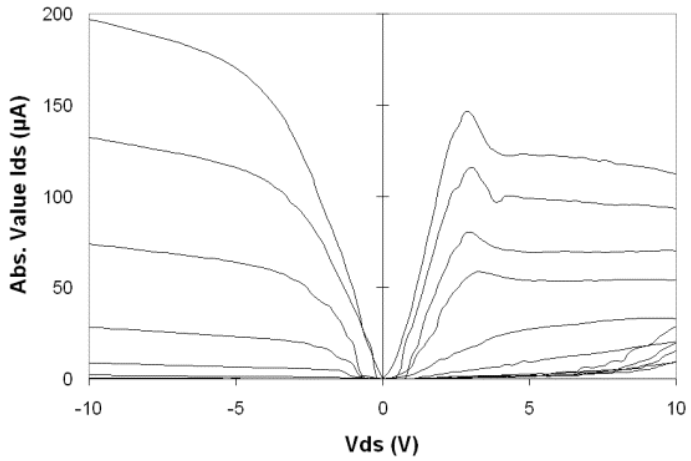

Fig. 9: Absolute value Ids vs. Vds characteristic for 2μm x 5μm n-body SFET from Wafer 6 after a 23 run burn-in. Vgs magnitude was varied from 0V to 10V, as in Fig. 9. This device was tested 2 months after the device in Figs.6-8. Peak current in the first quadrant is 146μA, and 197μA in the third quadrant. The first quadrant NDR region occurs at a lower drain bias than that in Fig. 6, which is attributed to a difference in barrier height (this will be discussed later in further detail).

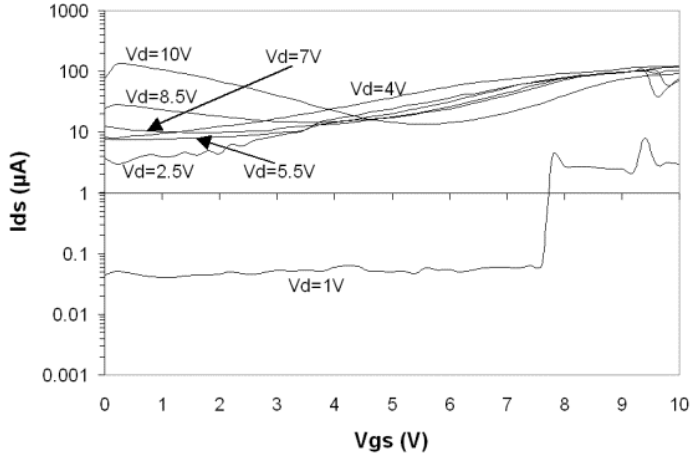

Fig. 10: Ids vs. Vgs characteristic for 2μm x 5μm n-body SFET (n-channel). Compared to Fig. 7 (the characteristics of which were fairly repeatable at the time of testing), n-channel gate control is degraded considerably, with a very small Ion:Ioff (~1 dec.) and very large sub-Vt slope (several Volts/dec.).

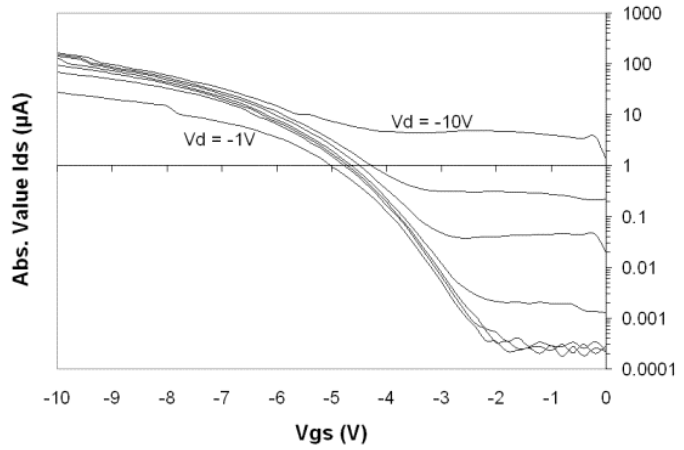

Fig. 11: Absolute value Ids vs. Vgs characteristic for 2μm x 5μm n-body SFET (p-channel). Vds was varied from –1V to –10V in –1.5V increments. Performance is considerably improved over the device in Fig. 8.

It is important to note that the n-channel and p-channel drive currents vary from die to die, due to the variance in surface states at the metal-silicon interfaces and charges in the TEOS gate dielectric for each FET (in either channel mode, however, current drive values of up to ~300+μA have been measured), which consequently affect the source/body and drian/body barrier heights, as well as the effective gate bias. Naturally, this results in a lack of drive current predictability, thus further supporting the case for using metal silicides as the source/drain material. In comparing Figs. 7 and 10, and 8 and 12, there is reason to believe that, for the device presented, accumulation mode (n-channel) operation degrades over time, while inversion mode (p-channel) operation improves. This can be attributed to a change in surface states at the metal-silicon interface, as well as the TEOS-silicon interface, which, respectively, affect the barrier heights and effective gate bias. Figs. 12-14 compare Vt, Ion:Ioff, and sub-Vt slope between the device in Figs. 5-8 (initial testing) and the device in Figs. 12-14 (testing after 2 month waiting period).

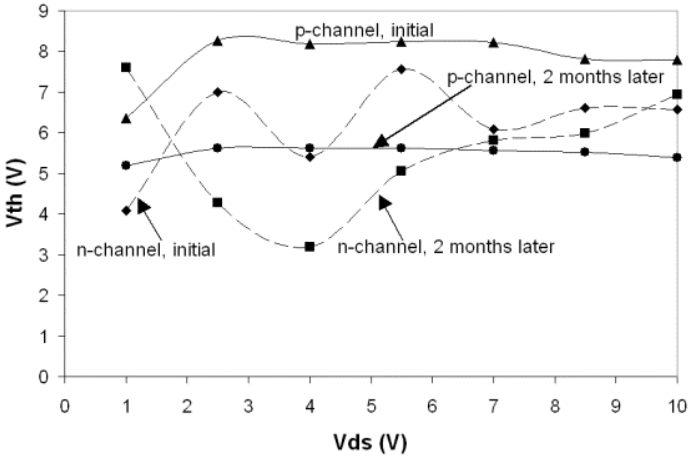

Fig. 12: Absolute value Vth vs. Vds (absolute value) for 2μm x 5μm n-body SFET, n-channel and p-channel operation.

As Fig. 12 shows, during first quadrant (n-channel) operation, Vth generally *increases* with Vds. This is because the increase in the size of the depletion region at the reverse biased diode results in body depletion, which results in an increase in the gate bias required to accumulate enough electrons for first quadrant operation to take place (though as Fig. 12 shows, first quadrant operation is rather erratic, the reasons of which are currently unkown). This also explains the decrease in Vth (albeit slight) with Vds for third quadrant (p-channel) operation. As Fig. 12 shows data from two separate devices, the change in the absolute value of Vth is not important, but rather the change in Vth dependence on Vds, which is smaller for p-channel operation for the device that was tested after 2 months. There does not appear to be enough stability in the n-channel operation to draw any conclusions regarding changes in Vth dependence on Vds.

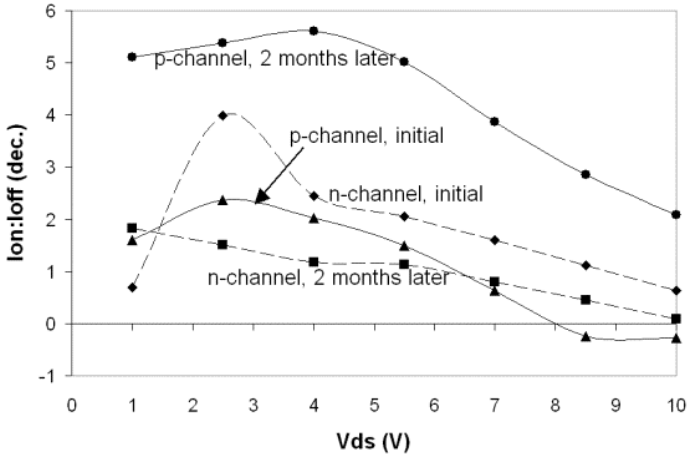

Fig. 13: Ion:Ioff vs. Vds (absolute value) for 2μm x 5μm n-body SFET, n-channel and p-channel operation. P-channel Ion:Ioff increased significantly over the 2 month period, mostly due to a decrease in p-channel leakage current dependence on Vds, while n-channel Ion:Ioff decreased significantly, mostly because of the increase in first quadrant leakage current.

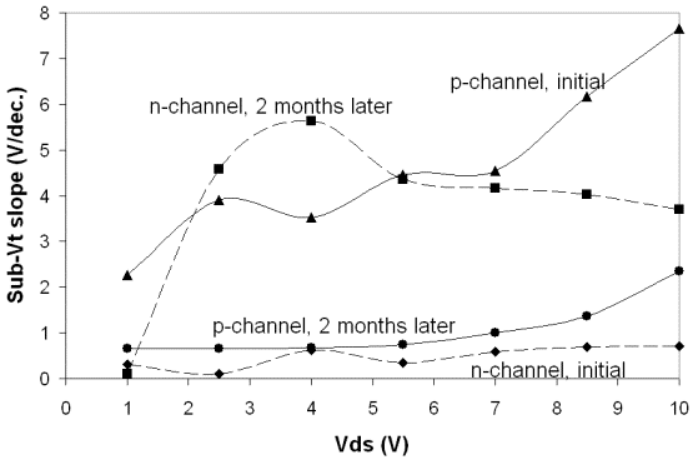

Fig. 14: Sub-Vt slope vs. Vds (absolute value) for 2μm x 5μm n-body SFET, n-channel and p-channel operation. Sub-Vt slope and Vds dependence for p-channel operation is considerably improved after 2 months (649mV/dec. at Vds = -1V). Interestingly enough, the best sub-Vt slope comes in the 2 months case in first quadrant operation at low Vds (109mV/dec. at Vds = 1V).

In examining Fig. 6, the electron leakage current during third quadrant operation is a result of DIST. This effect is not necessarily symmetrical about the y-axis, because under negative drain biases (but at low gate biases before inversion takes place), the drain/body diode is the reverse biased diode (and hence the current limiter). Under positive drain biases, while the source/body diode is the reverse biased diode, for zero gate bias the body region near the drain is inverted (due to the negative Vgd). This results in a reverse biased source/body diode with n-type Si in series with a reverse biased drain/body diode with p-type Si, which means that both electrons *and* holes are injected into the body region under large positive drain biases. Since holes see no barrier when traversing the reverse biased source/body n-Si Schottky diode, and vice versa, the leakage current for positive drain biases should be much larger than that of negative drain biases. This is shown by the leakage asymmetry in Fig. 9.

The reason why the leakage asymmetry is reversed in Fig. 6 (higher third quadrant leakage) could be attributed to a lower barrier height to n-Si for that device, which means more third quadrant source/body leakage and less first quadrant drain/body hole injection (a smaller barrier height to n-Si results in a larger inversion mode barrier height). This is illustrated in Figs. 15 and 16, which show first and third quadrant leakage, respectively, before and after a burn-in is performed. The burn-in is the same type of burn-in shown in Fig. 5, during which donor-like and acceptor-like surface states at the M-S interfaces fill up with electrons, ultimately resulting in more negative charge at the silicon side of the M-S junction. This increases the image force from the metal, thus decreasing the barrier height. Predictably, first quadrant leakage is lowered (the inversion mode drain/body barrier height is raised), while third quadrant leakage is increased in the form of thermionic emission.

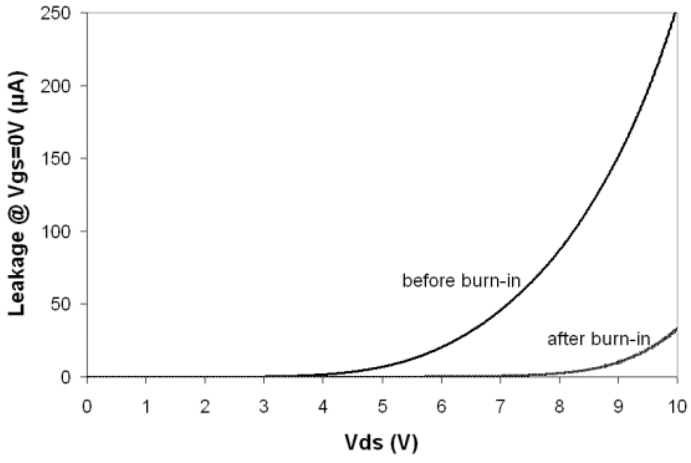

Fig. 15: First quadrant leakage current vs. Vds for 2µm x 5µm n-body SFET, before and after a burn-in process.

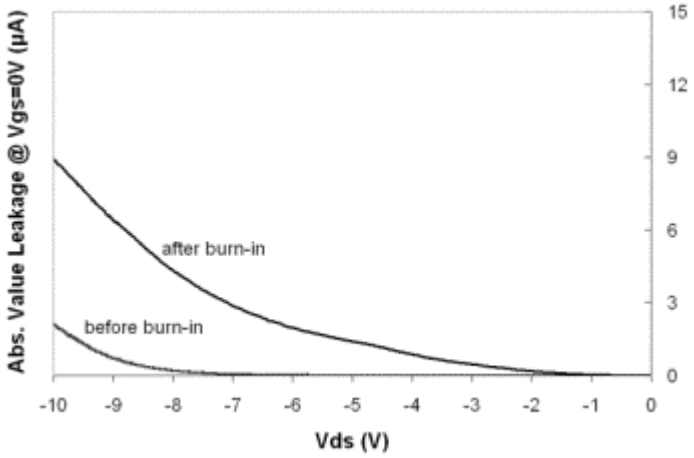

Fig. 16: Third quadrant leakage current (absolute value) vs. Vds for 2µm x 5µm n-body SFET, before and after a burn-in process.

Such a change in leakage current leads one to conclude that the sinter process performed during fabrication was ineffectual in its intended job of increasing the source/body and drain/body barrier heights. Typically, a "fresh" Schottky diode using Al and n-Si has a barrier height of 0.45eV, which increases to about 0.7eV over a period of a few months [10] (performing a sinter should result in a 0.7eV barrier height immediately), which is consistent with the empirical comparison between the device tested shortly after fabrication (Figs. 5-8) and the device tested 2 months later (Figs. 9-11).

Another characteristic shown in Figs. 6 and 9 is a negative differential resistance (NDR) region during first quadrant operation at elevated drain biases, which becomes stronger with increasing gate bias. This NDR characteristic varies from die to die, and is sometimes not even present (e.g., the saturation region is flat) in the 10V Vds range used for testing. Since first quadrant operation is limited by carrier injection through the source/body diode, most of the voltage drop takes place at the source. The field at the source cancels out the electron accumulation effect provided by the gate, which in turn pushes the Fermi band away from the conduction band and closer to the intrinsic band, thus *increasing* the barrier width. Consequently, the increase in barrier width results in a decrease in electron tunneling through the source/body diode (though thermionic emission remains), thus decreasing the measured drain current. A small barrier height to n-Si would result in a larger thermionic emission component, thus requiring a larger drain bias before the decrease in tunneling current makes an appreciable difference. This is shown in Fig. 6 at high drain biases, whereby previously discussed evidence suggests that the n-Si barrier height is lower than for the device in Fig. 9 (for which the NDR region occurs at a lower drain bias). This is also shown in Fig. 5, where the barrier height is at its largest during the first burn-in iteration, and decreases as surface states fill up, thus increasing the drain bias at which NDR is noticed.

At very large drain biases, the first quadrant leakage components previously discussed (DIST) begin to dominate

current flow. Predictably, larger gate biases increase the drain bias at which DIST takes place, due to the increase in accumulated electrons at the interface, as illustrated in Fig. 17.

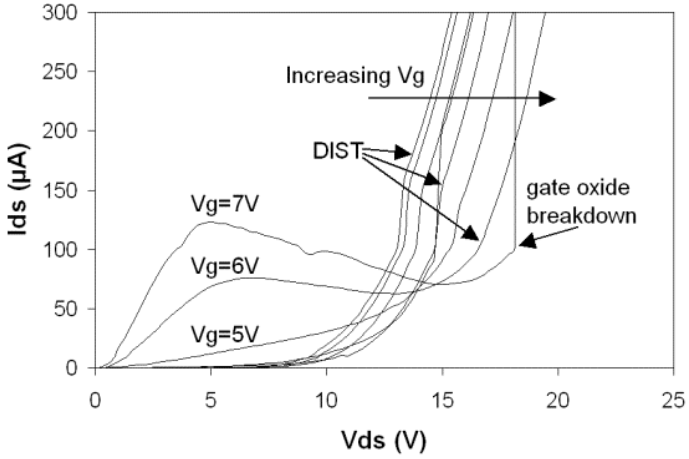

Fig. 17: Ids vs. Vds for 2μm x 5μm n-body SFET, taken to very high drain biases. Eventually, first quadrant leakage mechanisms begin to dominate current flow, though the drain bias at which this takes place can be increased with increasing gate bias.

In comparing the three sinter splits performed during fabrication, there is nothing to indicate that the different sinters had a different effect on device performance, but rather that the variations in performance are greater from wafer to wafer. This is illustrated in Figs. 18 and 19 for p-channel operation regarding Vth and Ion:Ioff, respectively. The idea behind the different sinter splits was that, since hydrogen is used in the forming gas sinter process, and since at various steps of fabrication different regions of the M-S interface are exposed, the degree of Si passivation would be different between the three splits. This would be an added effect, as the primary purpose of the sinter process is to increase the Al-Si barrier height to its maximum value, as mentioned previously. However, it appears that the 450°C sinter was not a high enough temperature to result in significant passivation, no less changes in the degree of passivation.

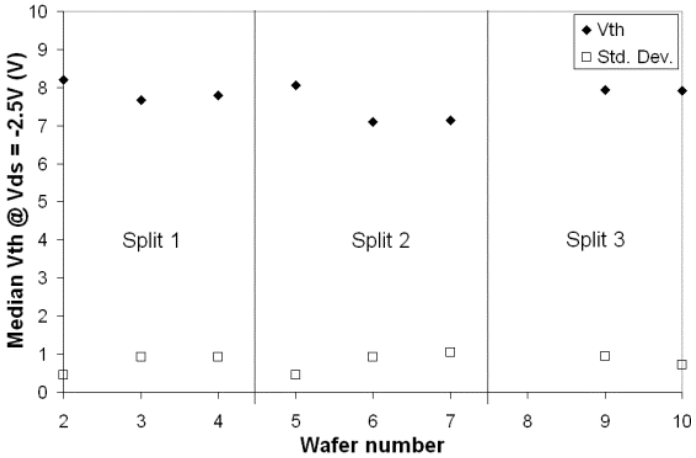

Fig. 18: Median Vth @ Vds = -2.5V and standard deviation vs. wafer number for 2μm x 5μm n-body SFET, p-channel operation. All devices on wafer 8 failed during testing. No appreciable difference exists between the three sinter splits.

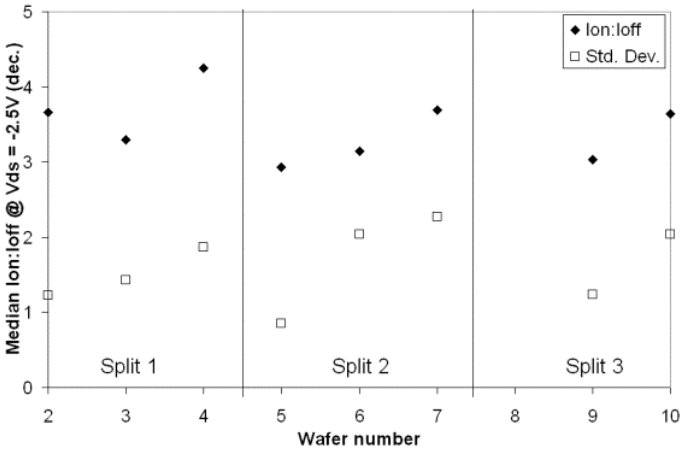

Fig. 19: Median Ion:Ioff @ Vds = -2.5V and standard deviation vs. wafer number for 2μm x 5μm n-body SFET, p-channel operation. Ion:Ioff variation is greater between wafers than between sinter splits.

P-body device operation is demonstrated in Fig. 20. That there is a measured Ids at Vds = 0V suggests some form of gate leakage, and it turns out that the p-body SFET is dominated *entirely* by gate leakage current. This observed leakage is highly repeatable in the p-body devices, which is interesting considering the thickness (500Å) of the gate dielectric. The post boron implant anneal (56min. at 1000°C) may have played a role in this, as a current path through the TEOS over the p-body regions would seem to be due to some type of defect propagation. Unfortunately, then, voltage transfer characteristics of the fabricated inverters could not be demonstrated.

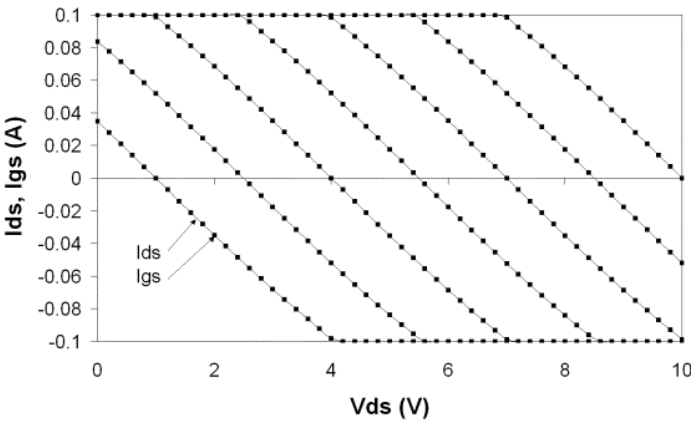

Fig. 20: Ids vs. Vds for 2μm x 5μm p-body SFET. The solid lines represent Ids, and the dotted lines represent Igs. Gate leakage current dominates device operation, and does now allow switching via gate-induced body depletion.

V. CONCLUSION

It was the purpose of this investigation to show that field effect transistors made of metal sources and drains can function via gate-modulated tunneling, thermionic emission, and body depletion. Gate-modulated tunneling and thermionic emission have been demonstrated in the n-body MSD SFET, and the results show potential for full CMOS

operation. Operation of the p-body device was dominated by gate leakage via defect propagation through the gate dielectric, so a higher quality gate dielectric would be necessary to demonstrate the device as it was intended to operate. It was also discussed that real-world Schottky CMOS design must consider more than just inversion mode operation, due to ambipolarity in Schottky source/drain devices. Multiple potential solutions for implementing Schottky CMOS have been conceived by the author, one of which was presented in this paper. Future work will involve fabricating a Schottky source/drain FinFET using metal silicides and demonstrating real-world Schottky CMOS operation.

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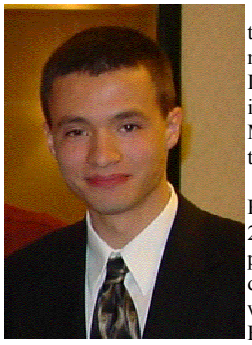

Reinaldo Vega became a Student Member of the IEEE in 2004. He received the B.S. degree in microelectronic engineering from the Rochester Institute of Technology in Rochester, New York in 2004, and is currently working towards the M.S. degree in microelectronic engineering from the Rochester Institute of Technology.

He joined Integrated Nano-Technologies in Rochester, New York during Summer/Fall of 2001 as a Co-op student, developing a fabrication process for prototype interdigitated DNA detectors. During Summer/Fall of 2002, he worked as a Co-op student at IBM in East Fishkill, New York, where he performed an analysis of RF MEMS and alternative power generation techniques, and worked on copper thru-plated inductors. He returned to IBM in Summer/Fall of 2003 as a Co-Op student, where he worked on SOI device characterization of thermal diodes, FETs, and electrically programmable fuses (eFUSE) at the 90nm technology node. During Spring of 2004, he performed a NSF Research Experience for Undergraduates, working on a multi-valued logic test setup and fabrication/circuit design for resonant interband tunnel diodes.

For his work in MSD SFETs, Mr. Vega received First Place in the 2004 RIT IEEE Student Design Contest. He is also a recipient of the 2004 Professor I. Renan Turkman Scholarship for Outstanding Achievements in Semiconductor Device Engineering and the 2004 RIT Undergraduate Research Symposium Award of Excellence.